Influence of the Technology on the Destruction Effects of Semiconductors by Impact of EMP and UWB Pulses

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Abstract
In this paper the influence of TTL- and CMOS-technology on the destruction effects of semiconductors by impact of EMP and UWB pulses is determined. Different logic devices like NANDs and inverter were exposed to high amplitude transient pulses.

Keywords
UWB, EMP, Susceptibility, TTL, CMOS, Semiconductor

I. INTRODUCTION
The goal of this investigation is to measure the susceptibility of electronic devices to a transient electromagnetic field threat. Modern electronics are of vital importance for the function of traffic systems, security systems and modern communication. A malfunction in one of these areas could cause casualties and economic disasters. Nowadays HPM and UWB equipment can be bought by everyone. Taken the aspect of electromagnetic terrorism into account an UWB system could be a very dangerous weapon, because it can be built in a very small volume due to the low energy content of the pulse. Therefore the susceptibility of electronics to pulsed electromagnetic fields like EMP and UWB pulses is of great interest. The intention of this work is to analyze the influence of the semiconductor technology on the breakdown and destruction effects. On that account ten different technologies (six TTL- and four CMOS-Technologies) have been tested. Upon destructions have occured the devices were opened and scanned with an electron microscope to analyze the effects which takes place on the different technologies.

II. GENERAL MEASUREMENT SETUP
The applied pulseshape is generally double exponential as shown in Figure 1. Five different pulse generating devices are available. Table 1 shows the rise time ($t_r$) and the full width half max value (fwhm) of the different pulses.

![Figure 1. Pulseshape and definitions](image)

Table 1. Pulse Data

<table>
<thead>
<tr>
<th>Pulse</th>
<th>Rise time $t_r$</th>
<th>fwhm</th>
</tr>
</thead>
<tbody>
<tr>
<td>UWB</td>
<td>100 ps</td>
<td>2.5 ns</td>
</tr>
<tr>
<td>EMP (fast)</td>
<td>1.5 ns</td>
<td>80 ns</td>
</tr>
<tr>
<td>EMP (med.)</td>
<td>5 ns</td>
<td>300 ns</td>
</tr>
<tr>
<td>UWB - slow EMP</td>
<td>500 ps - 10 ns</td>
<td>2.5 ns - 1600 ns</td>
</tr>
<tr>
<td>EMP (slow)</td>
<td>&gt;10 ns</td>
<td>500 ns</td>
</tr>
</tbody>
</table>

The measurements were carried out with two different waveguides shown in Figure 1 and 2. Waveguide 1 is an open area test simulator with a maximum height of about 23 m described in [1]. Waveguide 2 [2] is an open waveguide inside a shielded room enclosed by absorber walls. The absorbers at the end of the waveguide were placed on interchangeable wooden walls. The position of the septum can be adjusted via nylon threads. The measurements of the electromagnetic properties were done by a Time Domain Reflectometer (TDR) and electric and magnetic groundplane and free field probes as described in [3].
III. DEFINITIONS

III.1 Failure Rates
To describe the different failure effects two quantities have been defined [5]. The Breakdown Failure Rate (BFR) has been defined as the number of breakdowns of a system, divided by the number of pulses applied to it. A breakdown means no physical damage is done to the system. After a reset (self-, external- or power reset) the system is going back into function.

Table 2. Failure Rates

<table>
<thead>
<tr>
<th>Breakdown Failure Rate</th>
<th>Destruction Failure Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>BFR = ( \frac{\text{No. of Breakdowns}}{\text{No. of Pulses}} )</td>
<td>DFR = ( \frac{\text{No. of Destinations}}{\text{No. of Pulses}} )</td>
</tr>
</tbody>
</table>

The Destruction Failure Rate (DFR) of the device under test has been defined as the number of destructions divided by the number of pulses applied to the system. Destruction is defined as a physical damage of the system so that the system will not recover without a hardware repair.

III.2 Principle Behavior of BFR and DFR
The BFR and DFR behaviors in principle as shown in Figure 4. As important parameters for the description of the susceptibility of a system four quantities were defined.

IV. SUSCEPTIBILITY OF LOGIC-DEVICES
During the investigations ten different semiconductor technologies (six TTL-, four CMOS-families) have been tested (Table 3) concerning the susceptibility to EMP and UWB pulses. NANDs, inverter, generic array logic devices and shift registers were choosen to observe the influence of the technology on the destruction effects.

Table 3. Tested Technologies

<table>
<thead>
<tr>
<th>TTL-Technology</th>
<th>CMOS-Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard (S)</td>
<td>High Speed (HC)</td>
</tr>
<tr>
<td>Low Power Schottky (LS)</td>
<td>High Speed TTL-compatible (HCT)</td>
</tr>
<tr>
<td>Advanced Schottky (AS)</td>
<td>Advanced (AC)</td>
</tr>
<tr>
<td>Advanced Low Power Schottky (ALS)</td>
<td>Advanced TTL-compatible (ACT)</td>
</tr>
<tr>
<td>Fairchild Advanced Schottky (FAST)</td>
<td></td>
</tr>
</tbody>
</table>

IV.1 Test Setup
To apply the different pulses to the EUT a modular setup has been realized (Figure 5). Ten separate channels were built with a combination of differently printed circuit boards. The circuit boards were combined with ribbon cables to realize different coupling lengths at the input and output pins of the devices under test.
In Fig.6 a NAND test setup with 20 cm ribbon cable length at the input pins and ≈ 0 cm ribbon cable length at the output pins of the test devices is shown. The power supply is realized with ten different accumulators. DIP switches were implemented to the power supply unit to adjust arbitrary bit patterns at the input pins. LEDs and resistors were used as loads to observe the operating states of the devices.

### IV.2 Measurement Results

As a first result it can be noticed, that CMOS-devices first get reversible breakdowns which can be reversed by switching the power off and on again. At much higher field amplitudes non reversible destructions occur. This effect can be explained by a parasitic thyristor as a result of the vicinity of complementary n- and p-channel transistors in CMOS devices described in [5]. Figure 7 shows the BFR and DFR of NAND-devices built in four different CMOS technologies.

The comparison of CMOS- with TTL-NAND-devices shows, that the destruction thresholds are similar, but that TTL-NAND-devices only get non reversible destructions and at lower field amplitudes no breakdowns occurred (Figure 8) in contrary to the behavior of CMOS-NAND-devices.
Figure 9 shows the Breakdown- (BT) and Destruction threshold (DT) of NAND-devices built in ten different technologies (compare Table 3). The same effects were observed during the investigation of inverter devices.

![Figure 9. Breakdown (BT) and Destruction (DT) Threshold of CMOS and TTL NAND Devices](image)

**V. MICROSCOPIC ANALYSIS**

**V.1 Destruction Effects**

The microscopic analysis of the destructed devices generally shows three different damaging effects (Fig. 10). At lower field strengths only electronic components like diodes or transistors on the chip, mostly as a result of flashover effects, were damaged (Fig. 10a). If the amplitude of the electromagnetic pulse increases by about 50%, additional onchipwire destructions (this means smelting of pcb tracks without flashover effects) and multiple component destructions occurred (Fig. 10b). Further increase of the amplitude leads to additional bondwire destructions (Fig. 10c) and multiple component- and onchipwire-destructions.

![Figure 10. Destruction effects on chip level](image)

![Figure 11. NAND Device with multiple Destructions](image)

Similiar results were observed during the investigations of TTL-Inverter devices. Figure 12 shows the destruction failure rate (DFR) of TTL-Inverter devices, separated to component-, onchipwire- and bondwire-destructions. At the lowest field level component destructions occured. A further rising of the field strength resulted in onchipwire- and bondwire-destructions.

![Figure 12. DFR of TTL-NAND-Devices separated into Component- Bondwire- and Onchipwire-Destructions](image)

**V.2 Component Destructions**

Depending on the technology and the manufacturer, different component destruction effects have occoured. Figure 13 for example shows an 74S00 TTL NAND device with four component destructions after the impact of an EMP.
(tr = 7.5 ns,  fwhm = 180 ns, amplitude = 650 kV/m). All bondwires and onchipwires are intact.

Figure 13. Schottky-TTL NAND with Component-Destructions

Type 74xx00 devices are composed of four separate NAND gates with combined VCC and Ground pins. NAND 1 and 2 as well as NAND 3 and 4 are manufactured with symmetry to the x-y axis. At NAND 1 and 2 as well as NAND 3 and 4 the same components have been destructed. In Figure 14 and Figure 15 for example the damaged areas of NAND 1 and 2 is shown. Between point P1 and point P2, marked in Fig. 14-16, a flashover has occurred and as a result the metallic structure at the top layer directly around two distributed resistors (R1 and R2 in the depth of the material, not visible) has been destroyed and affected the two resistors.

Figure 14. Schottky -TTL NAND - Destruction in Detail

The fact, that always this area was damaged first, leads to the conclusion, that the damaged zone shown in Fig. 14 and 15 is the most susceptible area of the Schottky-TTL-NAND in this configuration and layout.

Figure 15. Schottky-TTL NAND - Destruction in Detail

Figure 16 shows the basic schematic of a Schottky TTL NAND device and the area where the flashover has occurred. At lower field strengths the resistors R1 and R2 have always been destructed first.

Figure 16. Schottky TTL NAND - Schematic

Similar effects were observed with the other technologies. The components on the chip, which were damaged first if the amplitude of the electromagnetic pulse was increased, are depending on the layout of the chip (and therefore on the manufactorer) as well as on the technology. Transistors, diodes and resistors were damaged similarly.

V.2 Onchipwire Destructions

A further rising of the amplitude of the electromagnetic pulse resulted in onchipwire destructions. Figure 17 shows different onchipwire destructions after the impact of an EMP with t_r = 7.5 ns, t_pulse = 180 ns and an amplitude of about 900 kV/m electrical field strength.
V.3 Bondwire Destructions

Bondwire destructions always occurred at higher pulse amplitudes than onchipwire destructions due to the fact that onchipwires normally have much lower cross sections than bondwires. The destructions occurred by melting of the material similar to onchipwire destructions. Figure 18 shows two destructed bondwires and pads.

The energy to destruct bond- or onchipwires can be calculated via the equation [5]

\[ Q = \rho \cdot A \cdot l \cdot c \cdot (T_{\text{melt}} - T_{\text{sur}}) \]  

(1)

with \( A \) = cross section, \( l \) = length of wire, \( \rho \) = density of material, \( c \) = specific heat capacity, \( T_{\text{melt}} \) = melting temperature and \( T_{\text{sur}} \) = surrounding area temperature. Equation 1 shows that the melting energy strictly depends on the cross section, if the same material is used for bond- and onchipwires under the constraint heat transfer into the surrounding area is negligible (valid due to short pulse impact). Drawing an energy balance results in equation 2 which allows to make a rough estimate of the current which was responsible for the bondwire destruction.

\[ I = \sqrt{\frac{\rho \cdot \kappa \cdot c \cdot \pi^2 \cdot d^4 \cdot (T_{\text{melt}} - T_{\text{sur}})}{16 \cdot \Delta t}} \]  

(2)

With \( \kappa \) = electrical conductivity, \( d \) = diameter of the bondwires and the assumption that the duration of the current is approximately equivalent to the pulse length, a current of \( I = 400 \, \text{A} \) can be calculated via equation 2 if bondwires made of aluminium were implemented.

VI. SUMMARY

The investigation of the susceptibility of logic devices built in ten different semiconductor technologies (NAND and Inverter) to EMP and UWB pulses has shown, that CMOS devices first gets reversible breakdowns and at much higher field amplitudes non reversible destructions occur. The destruction thresholds of TTL and CMOS devices are similar but TTL devices always gets non reversible destructions. The breakdown- (BT) and destruction-thresholds (DT) decreases much by extending the ribbon cable length or usage of pulses with faster rise times. The destruction effects can be separated into component- onchipwire- and bondwire-destructions. First, at lower field amplitudes, component destructions mostly as a result of flashover effects, occur. If the amplitude increases also onchipwire destructions appear. Further increase of the amplitude is leading to additional bondwire destructions and multiple component- and onchipwire-destructions.

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REFERENCES